REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 3-5 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Dye* (U.S. Patent No. 6,145,069). Applicant respectfully traverses this rejection.

Claims 1, 6, 16, 19, and 20 have been amended to add limitations that clarify Applicant's invention as claimed. Limitations have been added for the two separate buses that couple the RAM and the non-volatile memory to the processor and the third dedicated bus that connects the RAM with the non-volatile memory. Additionally, limitations have been added that make it clear that the RAM is separate from the non-volatile memory.

Applicant's arguments from previous response still apply in that *Dye* neither teaches nor suggests Applicant's invention as claimed. The amended claims make it clear that the non-volatile and volatile memories are separate and communicate over separate buses with the processor. The amended claims also make it clear that the volatile and non-volatile memories communicate over a dedicated bus only connecting those two memories.

Claim Rejections Under 35 U.S.C. § 103

Claims 2, 5-7, 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harari et al.* (U.S. Patent No. 6,266,724) in view of *Fallon* (U.S. Patent Application Publication No. 2002/069354). Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* (U.S. Patent No. 6,058,474) in view of *Iverson* (U. S. Patent No. 6,332,172). Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz* in view of Iverson and further in view of *Harari*. Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dye*, *Harari* and *Fallon*, and further in view of *Baltz*. Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz*, *Iverson* and *Harris* as applied to claim 16 above, and further in view of *Shin* (U.S. Patent No. 6,735,669). Applicant respectfully traverses this rejection.

Even if it were obvious to combine the cited references, and Applicant still maintains that it is not, there is no combination of *Dye*, *Harari et al.*, *Baltz et al.*, *Fallon*, *Iverson*, and/or *Shin* that would produce Applicant's invention as now claimed in the amended claims. None of these

references, either alone or in any combination disclose a processor coupled to a non-volatile memory over a serial bus and to a volatile memory over a separate, synchronous bus wherein the non-volatile and volatile memories are connected together over a dedicated third bus that connects only the two memories.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner withdraw the final rejection and allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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